ABSTRACT OF THE DISCLOSURE

A processor is contemplated which includes a queue configured to store one or more instructions and a control circuit coupled to the queue. The control circuit is configured to detect a replay of a first instruction due to a dependency on a load miss. In response to detecting the replay, the control circuit is configured to inhibit issuance of the one or more instructions in the queue to one or more pipelines of the processor. A carrier medium comprising one or more data structures representing the processor are also contemplated, as are a method of detecting the replay and inhibiting issuance of instructions in the queue in response to detecting the replay.